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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
QUILLEN, ALLEN E	

ART UNIT	PAPER NUMBER
2676	

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9

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/715,746	LEFEBVRE ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16,17 and 19-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16,17 and 19-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 1-4, 7-14, 17, 20-25 are amended, 26-37 added. Claims 15, 18 are cancelled. Claims 1-14, 16-17, 19-37 are pending. Applicant's arguments with respect to claims 1, 7, 11, 21, 25 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 2, 6-8, 11-12 are provisionally rejected under the judicially created doctrine of provisional obviousness-type double patenting as being unpatentable over claims 1, 7, 11 and 12 of copending Application No. 09/715253. Claims 3-5, 9-10, 13-14 are provisionally rejected under the judicially created doctrine of provisional obviousness-type double patenting as being unpatentable over claims 4, 7 and 9 of copending Application No. 09/715335. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented. The conflicting claims are not identical; they are patentably distinct from each other because current application 09/715,746 additionally recites "plurality of display devices". Applications No. 09/715253 and Application No. 09/715335 do not recite "plurality of display devices". At the time of the invention, it would have been obvious to one skilled in the art of computer graphics processing to use a plurality of displays to achieve a larger-sized display.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-4, 11-12, 16, 19, 21, 25-32, 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: http://www.rgb.com/Webpages/prodpgs/cwall.html, Firester et al, U.S. Patent 6,611,241, Pesto, Jr. et al, U.S. Patent 6,518,971, Kohli et al, U.S. Patent 6,252,600, and Deering, U.S. Patent 6,496,186.

6. Regarding claim 1, representative of claims 11, 21, MacInnis discloses a single graphical display system (Figures 1-7, 48, 60-64, 69-70, 73-74; Column 6, lines 21, 29-33), comprising: an interface configured to receive graphical data defining an image (Column 5, lines 7-20, 34-37, 45-49); and a plurality of graphical acceleration units (Figure 69, Column 112, lines 24-30, *four independent graphics conversion pipelines... speeds up graphics conversion process,* Figure 2,

element 64; Figure 37, element 64; *completely contained in an integrated chip,* Column 59, lines 10-12; *..the system may be implemented using two or more separate integrated circuit chips,* Column 61, lines 29-56), each of said plurality of graphical acceleration units respectively interfaced with one of said plurality of displays and configured to render a portion of said graphical data to said one display device such that said display displays said image as a single screen (*window descriptors, list,* Column 13, lines 1-33), wherein at least one of said graphical acceleration units comprises: a first graphical pipeline configured receive and process a graphical command (*LOAD,* Column 59, lines 21-34), said first graphical pipeline configured to render graphical data (Figure 69, Column 112, lines 24-33); a second graphical pipeline configured to receive and process said graphical command (see above, Column 108, lines 31-41; *xcnt, graphics controller, LINE_START,* Column 118, lines 5-10); and a compositor interfaced with said first and second graphical pipelines and one of said display devices (Column 115, lines 48-53).

MacInnis does not disclose a single logical screen (SLS) graphical display system comprising a plurality of display devices. RGB Spectrum Specification teaches the single logical screen (SLS) graphical display system comprising a plurality of display devices (*video wall*, page 1, lines 4-9). The motivation for combining graphics pipeline processing and video compositing with a video wall is for high resolution imagery for large display walls used in data assessment and decision making for real-time command, control and communications and control rooms (RGB Spectrum, page 1). RGB Spectrum Specification is evidence that, at the time of the invention, it would have been obvious for someone skilled in the art of graphical and video data digital display processing to combine the benefits of interfacing, pipeline processing using multiple pipelines and video compositing, as MacInnis discloses, with multiple displays, as

the RGB Spectrum Specification teaches, to provide for large video walls for data assessment and decision making.

Furthermore, Applicant discloses three-dimensional objects (Page 1, line 15), three-dimensional graphical data (Page 4, line 9), a single logical screen (SLS) with multiple display devices (Page 2, line 9 through Page 3, line 2); networked LAN interconnects (Figure 2, Page 3, line 20 through Page 4, line 4).

MacInnis does not disclose plurality of display devices. Firester teaches plurality of display devices as a logical display (Column 18, line 31) operating on a LAN distributed, X-windows, parallel graphics processors, that share portions of the image, environment (Figures 1, 2, 18, 19, Column 17, lines 30-50; Column 18, lines 5-41). The motivation for combining parallel pipeline pixel processing with plurality of display devices operating as a logical display is to create a large high-resolution (HDTV) display at a reasonable cost (Column 1, line 65; Column 2, lines 4-9) that handles the edge overlap pixel combinational problem (Column 2, lines 10-30). Firester is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing X-windowed, distributed 3D graphical processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with plurality of display devices operating as a logical display (in an X-window environment), as Firester teaches, to enable large high-resolution displays at reasonable cost.

MacInnis does not disclose a plurality of graphic accelerator units. Pesto teaches a plurality of graphic accelerator units having first and second parallel processors coupled to the plurality of display devices rendering a portion of 2D and 3D (*OpenGL*) graphical data (Column 1, lines 28-35, 45-51; Figures 1-4, 7, Column 3, lines 18-21, 42, 45-65). The motivation for

combining parallel pipeline pixel processing with plurality of graphical accelerators with parallel processors is for processing speed (Column 1, line 42; Column 2, lines 12-13; Column 6, lines 1-17) while maintaining ordered relationship during rendering of the portions (*strips*) of the 3D object ([Claim 21] Column 3, lines 18-22). Pesto is evidence that at the time of the invention, it would have been obvious for one skilled in art of designing distributed 3D graphical processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with plurality of graphical acceleration units having multiple, parallel processors, as Pesto teaches, for processing speed and synchronization of the 3D portions of the graphical image.

MacInnis does not disclose said graphical command. Kohli teaches said graphical command for context switching between 2D and 3D graphics pipeline for rendering to a [stereo, Column 4, lines 1-8, Figure 2, element 29] display using the X-Windows system (Figure 2, Column 1, lines 15-20, 32-33, 45-48, 54-61). The motivation for combining parallel pipeline pixel processing with a 2D and 3D graphical context command (in an X-Windows environment) is to enable context switching management of the 3D-to-2D and 2D-to-3D rendering requirements while using 3D clients (Column 1, 32-61; Column 2, lines 10-12; Column 8, lines 21-26). Kohli is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with 2D and 3D graphical command for context switching, as Kohli teaches, in order to meet the requirements of 2D and 3D windowing and rendering in an X-windows environment.

MacInnis discloses said first and second graphical pipelines but does not disclose a first graphical pipeline configured to receive and process a graphical command, said first graphical

pipeline configured to render graphical data from said graphical command; a second graphical pipeline configured to receive and process said graphical command. [Furthermore, regarding claim 21, rendering in parallel, 3D object] Deering teaches configured to receive, process and/or render (*pipelined, clipped, super-sampled 3D objects in portions in parallel*) (Figure 3, Column 11, lines 14-22; 40-48; Column 12, 17-20; 36-37; 44-48). The motivation for combining parallel pipeline pixel processing with receiving, processing and/or [parallel] rendering by pipeline is improve the display by reducing display artifacts of 2D and 3D rendering (Column 2, lines 61-63; Column 4, lines 11-19). Deering is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical parallel pipelined pixel processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with sending, receiving, processing, and/or rendering graphical data to reduce the graphics system bandwidth requirements (Column 11, lines 23-27) while improving image display.

7. Regarding claim 2, representative of claim 12, MacInnis discloses the system of claim 1, wherein: said first graphical pipeline is configured to mathematically combine a first offset (*upper and lower layers,* Column 48, line 35 through Column 49, line 10) with coordinate values included in said graphical data rendered by said first graphical pipeline; said second graphical pipeline is configured to mathematically combine a second offset with coordinate values included in graphical data rendered by said second graphical pipeline; and said compositor is configured to blend color values associated with corresponding coordinate values within said graphical data rendered by said first and second graphical pipelines (see above, Column 49, lines

1-17; *vector processor, mathematically, arithmetic,* Column 59, lines 20-28; Column 66, lines 37-45; Column 109, lines 21; Column 48, line 4; Column 16, line 60 through Column 17, line 6).

MacInnis explicitly discloses window (*window controller, window descriptors*) and screen (*blended graphics...displayed on a television,* Column 97, line 26] relative (first and second offsets) compositing in four parallel and separate pipelines (Figure 61, Column 96, lines 55-63; Column 97, lines 34-41; Column 98, lines 4-8). [Also, see Deering, Column 18, lines 10-12.]

8. Regarding claim 3, representative of claims 4, 27-30, 35, MacInnis discloses the system of claim 1, wherein said second graphical pipeline is configured to discard said graphical data rendered by said first graphical pipeline (see above, Figure 69, Column 112, lines 24-33; Column 8, lines 7-9; Column 16, lines 47-50; *pipeline clipping*, instant application prior art, Page 3, lines 3-12); MacInnis does not disclose discard without rendering. Deering discloses discard, discard without rendering, or discard and render (*Clipping refers to defining the limits of displayed image...*, Column 12, lines 17-19; Column 13, lines 28-32). The motivation for combining parallel pipeline pixel processing with clipping and rendering is to enable using clipped data in future panning and zooming image displays (Column 13, lines 30-32).

[Claim 35] MacInnis does not disclose 3D object. Deering teaches 3D object (Column 12, line 36). The motivation for combining 3D graphics processing with 3D object is to map primitives to a three-dimensional view port and coordinate system such that a correct perspective is obtained for display (Column 12, lines 32-37). Deering is evidence that at the time of the invention, it would have been obvious for one skilled in designing 3D pipelined displays using

3D processing, to combine the benefits of parallel pixel pipelined processing, as MacInnis discloses, with a 3D object, as Deering teaches, for correct perspective and display.

9. Regarding claim 16, representative of claims 19, MacInnis discloses the system of claim 1, further comprising a graphics application (*Direct Draw*, Column 62, lines 33-35), wherein each of the portions of said graphical data rendered by said plurality of graphical acceleration units is transmitted from said graphics application (Column 112, lines 24-33).

10. Regarding claim 25, representative of claims 26, 31-32, 34, 36, MacInnis discloses a single screen graphical display method, comprising: receiving a graphical data defining an image; displaying said image via a display device as a single screen; and for each of said display devices, rendering in parallel a different portion of said graphical data and compositing said rendered portion, wherein said rendering comprises rendering, in parallel for a single one of said display devices, at least a portion of a three dimensional graphical object via plurality of graphical pipelines.

MacInnis does not disclose plurality of display devices as a single logical screen. Firester teaches plurality of display devices as a logical display (Column 18, line 31) operating on a LAN distributed, X-windows, parallel graphics processors, that share portions of the image, environment (Figures 1, 2, 18, 19, Column 17, lines 30-50; Column 18, lines 5-41). The motivation for combining parallel pipeline pixel processing with plurality of display devices operating as a logical display is to create a large high-resolution (HDTV) display at a reasonable cost (Column 1, line 65; Column 2, lines 4-9) that handles the edge overlap pixel combinational

problem (Column 2, lines 10-30). Firester is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing X-windowed, distributed 3D graphical processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with plurality of display devices operating as a logical display (in an X-window environment), as Firester teaches, to enable large high-resolution displays at reasonable cost.

MacInnis does not disclose rendering in parallel, 3D object. Deering teaches configured to receive, process and/or render portions of a 3D object (*pipelined, clipped, super-sampled 3D objects in portions in parallel*) (Figure 3, Column 11, lines 14-22; 40-48; Column 12, 17-20; 36-37; 44-48). The motivation for combining parallel pipeline pixel processing with receiving, processing and/or [parallel] rendering by pipeline is improve the display by reducing display artifacts of 2D and 3D rendering (Column 2, lines 61-63; Column 4, lines 11-19). Deering is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical parallel pipelined pixel processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with sending, receiving, processing, and/or rendering 3D object as graphical data to reduce the graphics system bandwidth requirements (Column 11, lines 23-27) while improving image display.

[Claim 26, 31, 34, 36] MacInnis does not disclose graphical acceleration unit comprises an interface coupled to first and second pipeline via a first and second local area network (LAN), said interface transmits graphical command to pipelines. Firester teaches comprises an interface coupled to first and second pipeline via a first and second local area network (LAN), said interface transmits graphical command to pipelines (Column 18, lines 6-13). The motivation for combining parallel pipelined pixel processing using graphical accelerator with multiple LAN

connections for each first and second pipeline is to enable industry standard data transfer across the network (Figure 19, Column 18, lines 5-34). Firester is evidence that at the time of the invention, it would have been obvious to one skilled in the designing X-window 3D processors, to combine the benefits of parallel pixel pipeline processing, as MacInnis discloses, with multiple LAN's for first and second pipelines, as Firester teaches, to enable standardized data transfer across the network.

Claim Rejections - 35 USC § 103

11. Claims 5-7, 23-24, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: http://www.rgb.com/Webpages/prodpgs/cwall.html, Jenkins, U.S. Patent 6,111,582, and, in further view of Deering, U.S. Patent 6,496,186

12. Regarding claim 5, MacInnis discloses the system of claim 3, wherein said first graphical pipeline is further configured to super sample said graphical data rendered by said first graphical pipeline, and wherein said second graphical pipeline is further configured to super sample said graphical data rendered by said second graphical pipeline (see above, *post filtering, digitized analog video capture,* Column 5, lines 56-61; Column 9, lines 46-55).

MacInnis does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple pipelines (Column 60, lines 29-63); wherein said first and

second images define at least a portion of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors,* Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of available connection bandwidth and allow rapid synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

MacInnis does not disclose configured to super sample said graphical data rendered by said second graphical pipeline. Deering teaches configured to super sample to said graphical data rendered by said second graphical pipeline (Figure 3, *one or more,* Column 11, lines 2-11; 14-26; 40-50; Column 14, lines 19-33). The motivation for combining parallel pipeline pixel processing with super-samples rendered by pipeline is improve the display by reducing display artifacts of 2D and 3D rendering (Column 2, lines 61-63; Column 4, lines 11-19). Deering is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical parallel pipelined pixel processing machines, to combine the

benefits of parallel pipeline pixel processing, as MacInnis discloses, with super-samples rendered by pipeline to reduce the graphics system bandwidth requirements (Column 11, lines 23-27) while improving image display.

13. Regarding claim 6, MacInnis discloses the system of claim 5, wherein said compositor is configured to blend color values included in said graphical data rendered by said first and second graphical pipelines (see above, Column 16, lines 14-25; Figures 28-30, Column 10, line 41 through Column 11, line 39).

14. Regarding Claim 7, representative of claims 23-24, 33, MacInnis discloses a graphical display system, comprising: first rendering means for rendering graphical data from first graphical command received by said first rendering means, said first rendering means including a plurality of pipeline means for rendering, in parallel, said graphical data from said first graphical command and a compositing means for compositing said graphical data rendered by said first plurality of pipeline means, each of said first plurality of pipeline means configured to render at least a portion of said graphical data from said first graphical command; (see above, Figure 69, Column 112, lines 24-33); first display means for displaying a first image based on said composited portion; said one graphical acceleration unit; (see above, Column 52, lines 18-19).

MacInnis does not disclose single logical screen (SLS) graphical display system. RGB Spectrum Specification teaches the single logical screen (SLS) graphical display system comprising a plurality of display devices (video wall, page 1, lines 4-9). The motivation for

combining graphics pipeline processing and video compositing with a video wall is for high resolution imagery for large display walls used in data assessment and decision making for real-time command, control and communications and control rooms (RGB Spectrum, page 1). RGB Spectrum Specification is evidence that, at the time of the invention, it would have been obvious for someone skilled in the art of graphical and video data digital display processing to combine the benefits of interfacing, pipeline processing using multiple pipelines and video compositing, as MacInnis discloses, with multiple displays, as the RGB Spectrum Specification teaches, to provide for large video walls for data assessment and decision making.

MacInnis discloses multiple pipelines (Column 112, lines 24-33) but does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple pipelines (Column 60, lines 29-63); wherein said first and second images define at least a portion of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors,* Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of available connection bandwidth and allow rapid synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the

benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

MacInnis does not disclose second rendering means for rendering graphical data from a second graphical command received by said second rendering means, said second rendering means including a plurality of pipeline means for rendering, in parallel, said graphical data from said second graphical command and a compositing means for compositing said graphical data rendered by said second plurality of pipeline means, each of said second plurality of pipeline means configured to render at least a portion of said graphical data from said second graphical command; first display means for displaying a first image based on graphical data composited by said compositing means of said first rendering means; and second display means for displaying a second image based on graphical data composited by said compositing means of said second rendering means, wherein said first and second images define at least a portion of a single logical screen image. Deering teaches second rendering means for rendering graphical data from a second graphical command received by said second rendering means, said second rendering means including a plurality of pipeline means for rendering, in parallel, said graphical data from said second graphical command and a compositing means for compositing said graphical data rendered by said second plurality of pipeline means, each of said second plurality of pipeline means configured to render at least a portion of said graphical data from said second graphical command; first display means for displaying a first image based on graphical data composited by said compositing means of said first rendering means; and second display means for displaying a second image based on graphical data composited by said compositing means of

said second rendering means, wherein said first and second images define at least a portion of a single logical screen image (Column 10, line 61 through Column 11, line 50).

MacInnis does not disclose rendering in parallel. Deering teaches configured to receive, process and/or render portions of a 3D object (*pipelined, clipped, super-sampled 3D objects in portions in parallel*) (Figure 3, Column 11, lines 14-22; 40-48; Column 12, 17-20; 36-37; 44-48). The motivation for combining parallel pipeline pixel processing with receiving, processing and/or [parallel] rendering by pipeline is improve the display by reducing display artifacts of 2D and 3D rendering (Column 2, lines 61-63; Column 4, lines 11-19). Deering is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical parallel pipelined pixel processing machines, to combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with sending, receiving, processing, and/or rendering 3D object as graphical data to reduce the graphics system bandwidth requirements (Column 11, lines 23-27) while improving image display.

[Claims 23-24, 33] MacInnis does not disclose 3D object. Deering teaches 3D object (Column 12, line 36). The motivation for combining 3D graphics processing with 3D object is to map primitives to a three-dimensional view port and coordinate system such that a correct perspective is obtained for display (Column 12, lines 32-37). Deering is evidence that at the time of the invention, it would have been obvious for one skilled in designing 3D pipelined displays using 3D processing, to combine the benefits of parallel pixel pipelined processing, as MacInnis discloses, with a 3D object, as Deering teaches, for correct perspective and display.

Claim Rejections - 35 USC § 103

15. Claims 8-10, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: http://www.rgb.com/Webpages/prodpgs/cwall.html, Jenkins, U.S. Patent 6,111,582 Deering, U.S. Patent 6,496,186, and, in further view of Kohli, et al, U.S. Patent 6,252,600.

16. Regarding claim 8, representative of claims 9, 10, 13, 14, MacInnis discloses the system of claim 7, wherein each of said plurality of pipeline means of said first rendering means includes a means for mathematically combining a different offset to coordinate values included in said graphical data from said first graphical command, and wherein said compositing means of said first rendering means includes a means for blending color values associated with corresponding coordinate values within said graphical data from said first graphical command; [Claim 9] wherein said first rendering means includes a means for receiving an input identifying a coordinate range, and wherein one of said plurality of pipeline means of said first rendering means includes a means for discarding, based on said coordinate range, graphical data from said first graphical data command (see above; Figure 15, Column 31, lines 34-64; *vector processor, mathematically, arithmetic,* Column 59, lines 20-28; Column 66, lines 37-45; Column 109, lines 21; Column 48, line 4; Column 16, line 60 through Column 17, line 6).

MacInnis discloses multiple pipelines (Column 112, lines 24-33) but does not disclose multiple rendering means nor a second image or portion of the image. Jenkins teaches multiple pipelines (Column 60, lines 29-63); wherein said first and second images define at least a portion

of a image; second rendering means for rendering a respective second portion of said graphical data, said second rendering means including a plurality of pipeline means for rendering said second graphical data portion in parallel and a compositing means for compositing said second rendered portion (Figures 1-4, Figure 13A, *sub-images, being handled by one of the sub-image processors,* Column 17, lines 52-55). The motivation for combining multiple pipeline processing with multiple sub-images with respective rendering means is for efficient use of available connection bandwidth and allow rapid synchronization with broadcast event stream, load balancing, computational efficiency, level of detail and resolution suited to human needs (Column 114, lines 51-54, 63-63; Column 117, lines 1-6, 24, 38-40, 48-50, 63-67, Column 118, lines 1-9, 17-28, 36-38, 55-65). Jenkins is evidence that at the time of the invention it would have been obvious to one skilled in the art of computer graphics processing to combine the benefits of parallel pipeline processing, as MacInnis discloses, with multiple sub-images rendering, as Jenkins teaches, for performance and display efficiencies.

MacInnis does not disclose said first graphical command. Kohli teaches said first graphical command for context switching between 2D and 3D graphics pipeline for rendering to a [stereo, Column 4, lines 1-8, Figure 2, element 29] display using the X-Windows system (Figure 2, Column 1, lines 15-20, 32-33, 45-48, 54-61). The motivation for combining parallel pipeline pixel processing with a 2D and 3D graphical context command (in an X-Windows environment) is to enable context switching management of the 3D-to-2D and 2D-to-3D rendering requirements while using 3D clients (Column 1, 32-61; Column 2, lines 10-12; Column 8, lines 21-26). Kohli is evidence that at the time of the invention, it would have been obvious to one skilled in the art of designing distributed 3D graphical processing machines, to

combine the benefits of parallel pipeline pixel processing, as MacInnis discloses, with 2D and 3D graphical command for context switching, as Kohli teaches, in order to meet the requirements of 2D and 3D windowing and rendering in an X-windows environment.

MacInnis does not disclose a different offset to coordinate values. Deering teaches a different offset to coordinate values (*perturbed regular grid, limited to a predetermined range,* Column 19, lines 43-50; Column 20, lines 1-28). The motivation for combining parallel pixel pipeline processing, XY coordinates, offset with a different offset is to improve display, reduce artifacts for 2D and 3D displays with using super-sampling (Column 4, lines 11-18). Deering is evidence that at the time of the invention, it would have been obvious to one skilled in designing 3D displays, to combine the benefits of parallel pixel pipeline processing, as MacInnis discloses, with a different offset to coordinate values, as Deering teaches, to achieve improved display capabilities.

Claim Rejections - 35 USC § 103

17. Claims 17, 20, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over MacInnis, et al, U.S. Patent 6,573,905 in view of Computer Wall II, RGB Spectrum, Inc., Specifications, 950 Marina Village Parkway, Alameda, CA 94501, 9/2000, available on the world wide web at: http://www.rgb.com/Webpages/prodpgs/cwall.html, in further view of Deering, U.S. Patent 6,496,186, and Dachille, et al, GI-Cube: An Architecture for Volumetric Global Illumination and Rendering, SIGGRAPH/EUROGRAPHICS Workshop on Graphics Hardware, August 2000, Interlaken Switzerland, ACM Press, NY, NY, pages 119-128

18. Regarding claim 17, representative of claims 20, 22, MacInnis discloses the system of claim 2, wherein said first and second graphical pipelines, by respectively combining said first and second offsets with coordinated values in said graphical data rendered by said first and second graphical pipelines, offsets an image defined by said graphical data rendered by said first graphical pipeline with respect to an in image defined by said graphical data rendered by said second graphical pipeline such that said compositor defines a jitter enhanced image by blending said color values (*window descriptors, list,* Column 13, lines 1-33); [Claim 22, wherein one of said graphical acceleration units comprises a plurality of graphical pipelines, each of said graphical pipelines configured to mathematically combine a different offset to corresponding coordinate values of the graphical data portion rendered by said one graphical acceleration unit such that the compositor of said one graphical acceleration unit jitter enhances an image defined by said graphical data portion rendered by said one graphical acceleration unit (see above).

MacInnis does not disclose jitter enhanced. [Examiner takes notice that the use of the term "jitter" can have multiple distinct meanings, for example, (1) frame to frame "jiggling", an undesired effect, (see below, Deering, Column 15, lines 54-65), (2) creating special desired effects (see below, Deering, Column 2, lines 38-60), and (3) a graphics rendering image enhancement method as documented in the literature related to reducing aliasing, a stair-stepping effect along a smooth line or curve, caused by display method limitations (see Deering and Dachille below).]

MacInnis does not explicitly disclose wherein said compositor defines a jitter enhanced image ([instant application: *..each pipeline 56-59 adds a small offset to the coordinates of each pixel rendered by the pipeline... offsets...can be randomly generated by each pipeline and/or can*

be pre-programmed into each pipeline 56-59.. Page 29, lines 14-18]. Deering teaches supersampling and filtering in the context of Applicant's specification (Column's 8-20; Column 14, lines 19-34, 4041, 54-55, *perturbed, offset,* Column 18, lines 1-5; Column 19, lines 43-67) but does not use the term "jitter". The motivation for combining parallel pipeline processing of graphical images with sampling and filtering with random offset to the coordinates of each pixel rendered in the pipeline is for improved image quality, particularly realism in real-time systems (Deering, Column 2, lines 55-67; Column 3, line 1 through Column 4, line 19).

Dachille discloses the term "jitter" in the context of pipeline processing, and as Examiner understands Applicant Specification (Page 121, left column, second paragraph, line 9). The motivation for combining parallel pipeline processing of graphical images with sampling and filtering, as Dachille discloses (Page 121, lines 3-8), is improve the quality of the image (anti-aliasing). Dachille is evidence that at the time of the invention, it would have been obvious for one skilled in the art of graphics processing to combine the benefits of sampling and filtering, as MacInnis discloses, by "jittering" pixel coordinates, that is by using small random offsets, as Dachille teaches, to improve displayed image quality (anti-aliasing).

[Claim 22] MacInnis does not disclose 3D object. Deering teaches 3D object (Column 12, line 36). The motivation for combining 3D graphics processing with 3D object is to map primitives to a three-dimensional view port and coordinate system such that a correct perspective is obtained for display (Column 12, lines 32-37). Deering is evidence that at the time of the invention, it would have been obvious for one skilled in designing 3D pipelined displays using 3D processing, to combine the benefits of parallel pixel pipelined processing, as MacInnis discloses, with a 3D object, as Deering teaches, for correct perspective and display.

Response to Arguments

19. Applicant's arguments with respect to claims 1, 7, 11, 21, 25 have been considered but are moot in view of the new ground(s) of rejection. Applicant has made extensive amendments to the claims and has added new claims forcing additional search and lengthy consideration, thus new grounds for rejection.

20. Applicant asserts MacInnis does not disclose graphical acceleration units, first graphical pipeline receives and processes a graphical command and renders data from this command, and that the second graphical pipeline receives and processes this command (Page 15, 1st Paragraph); MacInnis does not appear to render graphical data from the same graphical command, but by windows, thus the commands are independent of one another (Page 15, 1st Paragraph through Pge 16, 1st Paragraph); MacInnis fails to disclose each pipeline renders a portion of the graphical data (Page 17, 1st Paragraph; Page 18, 2nd Paragraph); MacInnis fails to disclose rendering in parallel, at least a portion of a 3D object (Pages 19-21).

21. The Examiner respectfully replies, however, that, in the claims, as now amended, MacInnis in combination with Firester, Kohli, Pesto, Deering discloses all features of Applicant's claimed invention. Firester teaches parallel processing to interpret graphics commands and process sub-image data for only the respective sub-image or portions of the displayed image using parallel processing (Figure 18, Column 17, lines 30-50) in an X-windows environment (Figure 19, Column 18, lines 5-41). Kohli teaches graphics systems employing 2D and 3D images using display windows in client server, X-Windows environment (Column 1-2) emphasizing the importance of the context switching command for rendeing either 2D X-

windows commands and graphics data, or 3D graphical data. Pesto teaches multiple parallel graphical accelerators processing different portions of 2D and 3D graphical data using OpenGL@ with parallel rendering (Column 1, lines 25-36, 45-52; Column 2, lines 1-14; Column 3, lines 19-21, 42, 45-65). Deering teaches the XY coordinate offsets used in antialiasing using super-sampling, multiple parallel rendering pipeline processors receiving graphical commands and clipping to retain, discard, render 3D objects (Column 17 through Column 21, line 23; Column 9-14) in a client-server environment.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to:

(703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

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January 10, 2004

Matthew C. Bella

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